W800 Specification

V2.0

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Document History

Version	Date	Revision Record	Author	Auditor
V0.1	2019/9/25	Initial Release	Ray	
V0.2	2020/3/24	Modify Function Information	Chengsheng	
V0.3	2020/5/9	Modify Performance Parameter	Ray	
V0.4	2020/5/15	Modify BT Parameter	Ray	
V0.5	2020/5/28	Update function description	Ray	
V2.0	2020/9/1	Add function description	Ray	

Content

1 General Description

W800 is a secure IoT Wi-Fi/Bluetooth SoC chipset. It complies 2.4G IEEE802.11b/g/n Wi-Fi protocol; supports BT/BLE working mode with BT/BLE4.2 protocol. W800 integrates 32bit CPU, UART, GPIO, SPI, SDIO, ADC, I^2C, I^2S, 7816, Touch Sensor etc. W800 supplies TEE security engine and multiple hardware enrcytion and decryption protocol. Integrates DSP, floating-point arithmetic unit. It integrates 2Mbyte Flash memory, supports multiple security measures such as firmware encryption storage, firmware signature, security debugging, security upgrade, etc. to ensure product safety features. W800 can be easily applied to smart home, smart appliance, wireless audio & video, smart toy, industry, health care and other IoT fields.

2 Features

- Chipset Packaging
  - ✓ Package QFN32, 4mm x 4mm
- MCU Features
  - ✓ Integrated 32bit XT804 CPU with max 240MHz. Integrated DSP, floating-point arithmetic unit and security engine.
  - ✓ Integrated 2MB Flash, 288KB RAM
  - ✓ Integrated Ex-PSRAM with max 64MB
  - ✓ Integrated 5 UART interface with max baud rate 2Mbps
  - ✓ Integrated 2 channel 16bit ADC with max sampling rate 1KHz
  - ✓ Integrated 1 High-speed SPI with max 50MHz
  - ✓ Integrated 1 SDIO_HOST interface, support SDIO2.0, SDHC, MMC4.2
  - ✓ Integrated 1 SDIO_DEVICE, support SDIO2.0
  - ✓ Integrated 1 I^2C controller
  - ✓ Integrated GPIO controller with max 18 GPIO
  - ✓ Integrated 5 channel PWM
  - ✓ Integrated 1 Duplex I^2S controller
  - ✓ Integrated 11 Touch Sensor
- Security Features
  - ✓ Integrated Tee security engine
  - ✓ Integrated SASC/TIPC. Memory and internal modules/interfaces can be configured with security attributs to prevent non-secure code access.
  - ✓ Enable the firmware signature mechanism to achieve secure boot/upgrade.
  - ✓ Support firmware encryption function, enhance code security
  - ✓ Firmware encryption keys are distributed using asymmetric algorithms to enhance key security

- ✓ Hardware encryption moduels: RC4256, AES128, DES/3DES, SHA1/MD5, CRC32, 2048 RSA, true random number generator

■ Wi-Fi Features

- ✓ Support GB15629.11-2006, IEEE802.11 b/g/n
- ✓ Support Wi-Fi WMM/WMM-PS/WPA/WPA2/WPS
- ✓ Support EDCA channel access
- ✓ Support 20/40M bandwidth
- ✓ Support STBC, GreenField, Short-GI and reverse transmission
- ✓ Support AMPDU, AMSDU
- ✓ Support IEEE802.11n MCS 0~7, MCS32, transmission rate is up to 150Mpbs
- ✓ Support Short Preamble in 2/5.5/11Mbps
- ✓ Support HT-immediate Compressed Block Ack, Normal Ack, No Ack
- ✓ Support CTS to self
- ✓ Support Station, Soft-AP, Soft-AP/Station function

■ BT Features

- ✓ Integrated BT baseband processor/ protocol processor
- ✓ Support BT/BLE dual-mode and support BT/BLE4.2 protocol

■ Power supply and consumption

- ✓ 3.3V single power supply
- ✓ Support Wi-Fi PS-mode
- ✓ Support working, Sleep, Standby etc modes
- ✓ Standby consumption <10 uA

3 Chipset Block Diagram

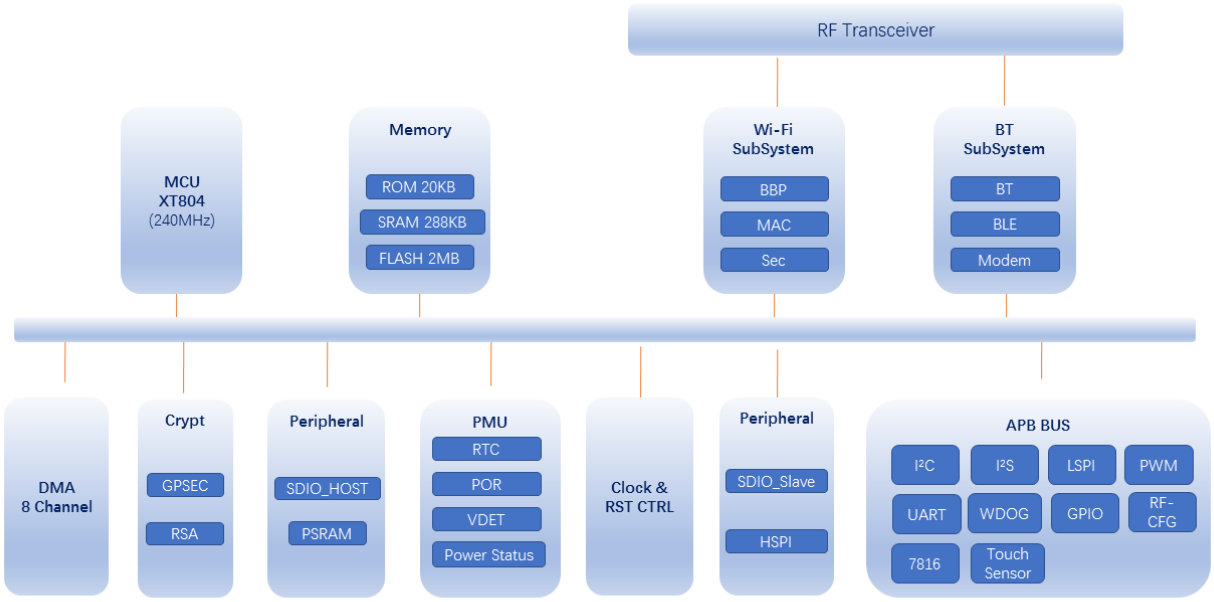

Figure3-1 W800 Block Diagram

4 System Memory Map

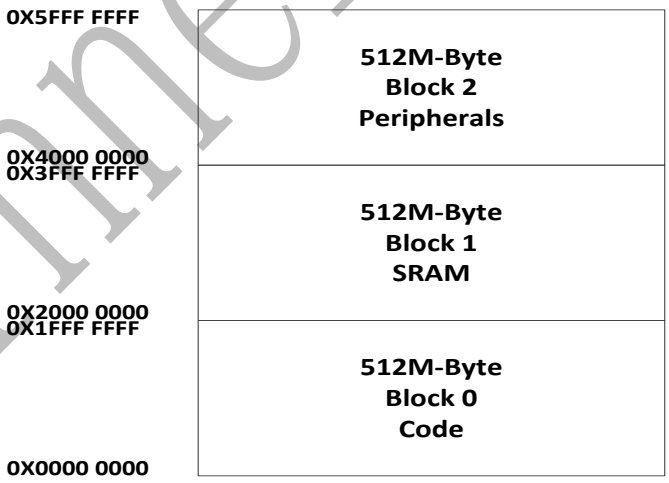

Figure4-1 Address Space Assignments

Table4-1 Peripheral Address Space Assignments

Peripheral	BootMode=0	Address Space	Description
ROM	0x0000 0000 ~ 0x0004 FFFF		Firmware

FLASH	0x0800 0000 ~ 0x0FFF FFFF		Specific Instruction Memory Space
SRAM	0x2000 0000 ~ 0x2002 7FFF		Firmware and Instruction Memory Space
Mac RAM	0x2002 8000 ~ 0x2004 7FFF		SDIO/H-SPI/UART data buffer
PSRAM	0x3000 0000 ~ 0x30800000		Peripheral Memory
CONFIG	0x4000 0000 ~ 0x4000 2FFF	0x4000 0000 ~ 0x4000 05FF	RSA
		0x4000 0600 ~ 0x4000 07FF	GPSEC
		0x4000 0800 ~ 0x4000 09FF	DMA
		0x4000 0A00 ~ 0x4000 0CFF	SDIO_HOST
		0x4000 0D00 ~ 0x4000 0DFF	PMU
		0x4000 0E00 ~ 0x4000 0EFF	Clock & Reset
		0x4000 0F00 ~ 0x4000 0FFF	MacPHY Router
		0x4000 1000 ~ 0x4000 13FF	BBP
		0x4000 1400 ~ 0x4000 17FF	MAC
		0x4000 1800 ~ 0x4000 1FFF	SEC
		0x4000 2000 ~ 0x4000 21FF	FLASH Controller
		0x4000 2200 ~ 0x4000 23FF	PSARM_CTRL
		0x4000 2400 ~ 0x4000 25FF	SDIO Slave
		0x4000 2600 ~ 0x4000 27FF	H-SPI
		0x4000 2800 ~ 0x4000 29FF	SD Wrapper
		0x4000 2A00 ~ 0x4000 A9FF	BT Core
		0x4000 B000 ~ 0x4000 B0FF	SASC-B1 Primary Bus Memory Security Configuration Module
		0x4000 B100 ~ 0x4000 B1FF	SASC-Flash Flash Security Configuration Module
		0x4000 B200 ~ 0x4000 B2FF	SASC-B2 Secondary Bus Memory Security Configuration Module
APB	0x4001 0000 ~ 0x4001 C000	0x4001 0000 ~ 0x4001 01FF	I^2C master
		0x4001 0200 ~ 0x4001 03FF	Sigma ADC
		0x4001 0400 ~ 0x4001 07FF	SPI master
		0x4001 0600 ~ 0x4001 07FF	UART0

		0x4001 0800 ~ 0x4001 09FF	UART1
		0x4001 0A00 ~ 0x4001 0BFF	UART2
		0x4001 0C00 ~ 0x4001 0DFF	UART3
		0x4001 0E00 ~ 0x4001 0FFF	UART4
		0x4001 1000 ~ 0x4001 11FF	
		0x4001 1200 ~ 0x4001 13FF	GPIO-A
		0x4001 1400 ~ 0x4001 15FF	GPIO-B
		0x4001 1600 ~ 0x4001 17FF	WatchDog
		0x4001 1800 ~ 0x4001 19FF	Timer
		0x4001 1A00 ~ 0x4001 1BFF	RF_Controller
		0x4001 1C00 ~ 0x4001 1DFF	
		0x4001 1E00 ~ 0x4001 1FFF	PWM
		0x4001 2000 ~ 0x4001 22FF	I²S
		0x4001 2200 ~ 0x4001 23FF	BT-modem
		0x4001 2400 ~ 0x4001 25FF	Touch Sensor
		0x4001 2600 ~ 0x4001 25FF	TIPC Interface Security Configuration
		0x4001 4000 ~ 0x4000 BFFF	RF_BIST DAC TX Memory
		0x4001 C000 ~ 0x4003 BFFF	RF_BIST ADC RX Memory
		0x4001 3C00 ~ 0x5FFF FFFF	RSV

5 Function Description

5.1 SDIO HOST Controller

The SDIO Host controller provides a digital interface that can access SD card and MMC card. Can be compatible with SDIO 2.0 protocol. There are CK, CMD and 4 data lines.

- Compatible with SD card specification 1.0/1.1/2.0(SDHC)
- Compatible with SDIO memory card specification 1.1.0
- Compatible with MMC specification 2.0~4.2
- Configurable interface clock rate, support host rate 0~50MHz
- Support standard MMC interface
- Support soft reset function
- Automatic Command/Response CRC generation/check
- Automatic data CRC generation/check

- Configurable timeout detection
- Support SPI, 1-bit SD and 4-bit SD modes
- Support DMA data transmission

5.2 SDIO Device Controller

The SDIO2.0 device-side interface to complete the data transimmision with host. Integrates 1024Byte asynchronous FIFO, completes the data interaction between the host and chipset.

- Compatible with SD card specification 2.0
- Support host speed 0~50MHz
- Support blocks up to 1024bytes
- Support soft reset function
- Support SPI, 1-bit SD and 4-bit SD modes

5.3 High-speed SPI Controller

- Compatible with general SPI protocol
- Optional level interrupt signal
- Support up to 50Mbps rate
- Simple frame format, full hardware analysis and DMA

5.4 DMA Controller

Support 8 channel, 16 DMA request signals, has chain table and register configuration

- Support Amba2.0 protocol, 8 channel DMA
- Support chain table operation mode
- 16 configurable DMA request signals
- Support 1, 4-burst data transfer
- Support byte, half-word, word-access
- Programmable source or destination address unchanged, sequentially increases or pre-defined
- Synchronous DMA request and DMA response timing

5.5 Clock and Reset Controller

Support the controller of clock and reset system. Clock controller include clock frequency

conversion, clock turn off and adaptive gating, and reset controller includes soft reset control of system and sub modules.

5.6 Memory Controller

Support the cache size configuration during transmitting and receiving, MAC access base address, cache number and frame aggregation control signals.

5.7 BBP

Support IEEE802.11a/b/g/e/n (1T1R). Mainly parameters:

- Data rate: 1~54Mpbs(802.11a/b/g), 6.5~150Mbps(802.11n)
- MCS data format: MCS0~MCS7, MCS32(40MHz HT Duplicate mode)
- Support 40MHz bandwidth non-HT Duplicate mode, 6M～54M
- Signal bandwidth: 20MHz, 40MHz
- Modulation mode: DSSS(DBPSK,DQPSK,CCK) and OFDM(BPSK,QPSK,16QAM,64QAM)
- Support 1T1R MIMO-OFDM spatial multiplexing
- Support Short GI mode
- Support legacy mode and Mixed mode
- Support data transmission and reception on 20M upper and low side in 40MHz bandwidth
- Support STBC receive with MCS0～7, 32
- Support Green Field mode

5.8 MAC Controller

Support IEEE802.11a/b/g/e/n MAC protocol. The mainly features:

- Support EDCA channel access
- Support CSMA/CA, NAV and TXOP protection mode
- Support Beacon, Mng, VO, VI, BE, BK and QoS
- Support unicast, broadcast and multicast TX/RX
- Support RTS/CTS, CTS2SELF, Normal ACK, No ACK frame format
- Support retry and control of power and transmission rate
- Support MPDU and Immediate BlockAck mode
- Support RIFS, SIFS, AIFS
- Support reverse transmission
- Support programmable TSF Timer
- Support MIB statistical information

5.9 Security System

Support IEEE802.11a/b/g/e/n protocol. Encryption or decryption in the process of transmitting and receiving data frames.

- Suppport throughput more than 150Mbps
- Support standard Amba2.0 bus protocol

- Support WAPI2.0
- Support WEP-64
- Support WEP-128
- Support TKIP
- Support CCMP

5.10 FLASH Controller

- Provide bus access in Flash interface
- Proved arbitration between system bus and data bus
- Implementation of CACHE
- Support compatible with different QFlash

5.11 RSA Encrytion

RSA, arithmetic hardware coprocessor, provides Montgomery (FIOS) modular multiplication. The module implements of RSA algorithm with RSA software library, and supports from 128-bit to 2048-bit.

5.12 Universal Hardware Encrytion Module

The specified length data in the source address will be automatically en-/decrypted, and the result data will be written to the designated destination address apace. The Module spports SHA1/MD5/RC4/DES/3DES/AES/CRC/TRNG。

- Support SHA1/MD5/RC4/DES/3DES/AES/CRC/TRNG
- Support ECB and CBC with DES/3DES
- Support ECB, CBC, CTR with AES
- Support CRC8, CRC16_MODBUS, CRC16_CCITT, CRC32 with CRC
- Support input/output reverse with CRC
- SHA1/MD5/CRC support continuous multi-packet encryption
- Built-in true random number generator, also supports seed to generate pseudo-random number

5.13 I²C Controller

I²C controller connects though APB interface. It supports master mode and configurable operating frequency (100K~400K).

5.14 Master/Slave SPI controller

Supports Master/Slave operating frequency is the frequency of system bus. The maily feature of the bus are:

- Provides separate 8-level depth transmit and receive FIFO buffers

- Support Motorola SPI protocol (CPOL, CPHA), Ti protocol, microwire protocol in master mode
- Support Motorola SPI protocol (CPOL, CPHA) in slave mode
- Suport full duplex and half duplex
- Support data length up to 65535bit in master mode
- Support data transfer of any bit length in slave mode
- 1/6 system clock frequency is max frequency of SPPI_Clk in slave mode

5.15 UART Controller

- Support APB bus protocol
- Support Interrupt or polling
- Support DMA, Separate reveive/transmet 32bytes enty FIFO buffer
- Programmable baud rate
- Programmable number of data bit, 5-8bit, and parity bit
- Programmable stop bit, 1 or 2
- Support RTS/CTS flow control
- Support Break frame
- Support interrupt of Overrun, parity error, frame error, rx break frame
- Up to 16-burst byte DMA data transfer

5.16 GPIO Controller

Programmable input and output, configurable interrupt. GPIOA and GPIOB have the same functionwith different base address.

5.17 Timer Controller

Configurable μS or mS Timer, has 6 programmable 32-bit timer. Use interrupt flag to detect time out.

5.18 Watchdog Controller

The watchdog is used to perform a system reset when system runs into an unknown state. The system software must respond to a periodic interruption, otherwise a hardware reset will be generated.

5.19 RF Configurator

Support SPI bus protocol. The operating clock is system clock. The mainly feature of the bus is:

- Provides separate 1-word depth transmit and receive FIFO buffer

5.20 RF Transceriver

- The RF transceiver includes a power amplifier, a transmission channel, a receiving channel, a phase locked loop and a SPI, which changes the working state of the chipset by the signals SHDN, RXEN and TXEN

- The receiving channel uses the zero intermediate frequency structure to convert the RF signal directly to the baseband I and Q output. The RF front end works in 2.4GHz, including low noise amplifier and orthogonal mixer. The baseband is composed of low pass filter and variable gain amplifier to realize channel filtering and gain control. The drive amplifier provides different DC output for the ADC interface
- The transmission channel includes programmable control filter, upcoverter mixer, variable gain amplifier and power amplifier. The transmission channel uses the output signal of direct frequency conversion structure. DAC signal through low pass filter, filter out the mirror frequency and out of band noise. PA output signal is different output to driver antenna

5.21 PWM Controller

- Support 5 channels PWM generators
- Support 2 channels input capture (PWM0 and PWM4)
- Frequency range: 3Hz~160KHz
- Duty ratio precision: 1/256, Dead-Zone counter: 8bit

5.22 I²S Controller

- Support APB bus protocol with 32bit single reading/writing operation
- Support Master/Slave, support full duplex
- Support 8/16/24/32 bit word size, sampling frequency is up to 128KHz
- Support mono and stereo audio data
- Support I²S and MSB justified data format, support PCM A/B data format
- Support DMA data transfer, word access only

5.23 7816/UART Controller

- Support APB bus protocol
- Support interrupt or polling
- Support DMA, separate receive/transmit 32 bytes entry FIFO buffer
- Support DMA data transfer, word access only. Up to 16-burst byte DMA data transfer

Support UART and 7816 feature:

UART feature:

- Programmalbe baud rate
- Programmable number of data bit, 5-8bit, and parity bit
- Programmable stop bit, 1 or 2
- Support RTS/CTS flow control
- Support Break frame
- Support interrupt of overrun, parity error, frame error, rx break frame

7816 feature:

- Support ISO-7816-3 T=0.T=1
- Support EVM2000 protocol
- Support guard time (11 ETU-267 ETU)
- Programmable inverse convention or direct convention
- Support receive/transmit data frame with prarity bit and retrans

- Programmable stop bit, 0.5 or 1.5

5.24 PSRAM Controller

Integrated PSRAM controller with SPI/QSPI interface, supports external PSRAM device access, and provides bus-based PSRAM read/write operations. The maximum reading and writing speed is 80MHz.

- Support read and write access to external PSRAM
- Configurable SPI or QSPI
- Configurable SPI/QSPI clock frequency
- Support BURST INC mode access
- Support semi-sleep mode of PSRAM

5.25 Touch Sensor Controller

- Support up to 11 Touch Sensor scanning
- Record the scan results of each Touch Sensor
- Report scan results through interruption

6 Pin Description

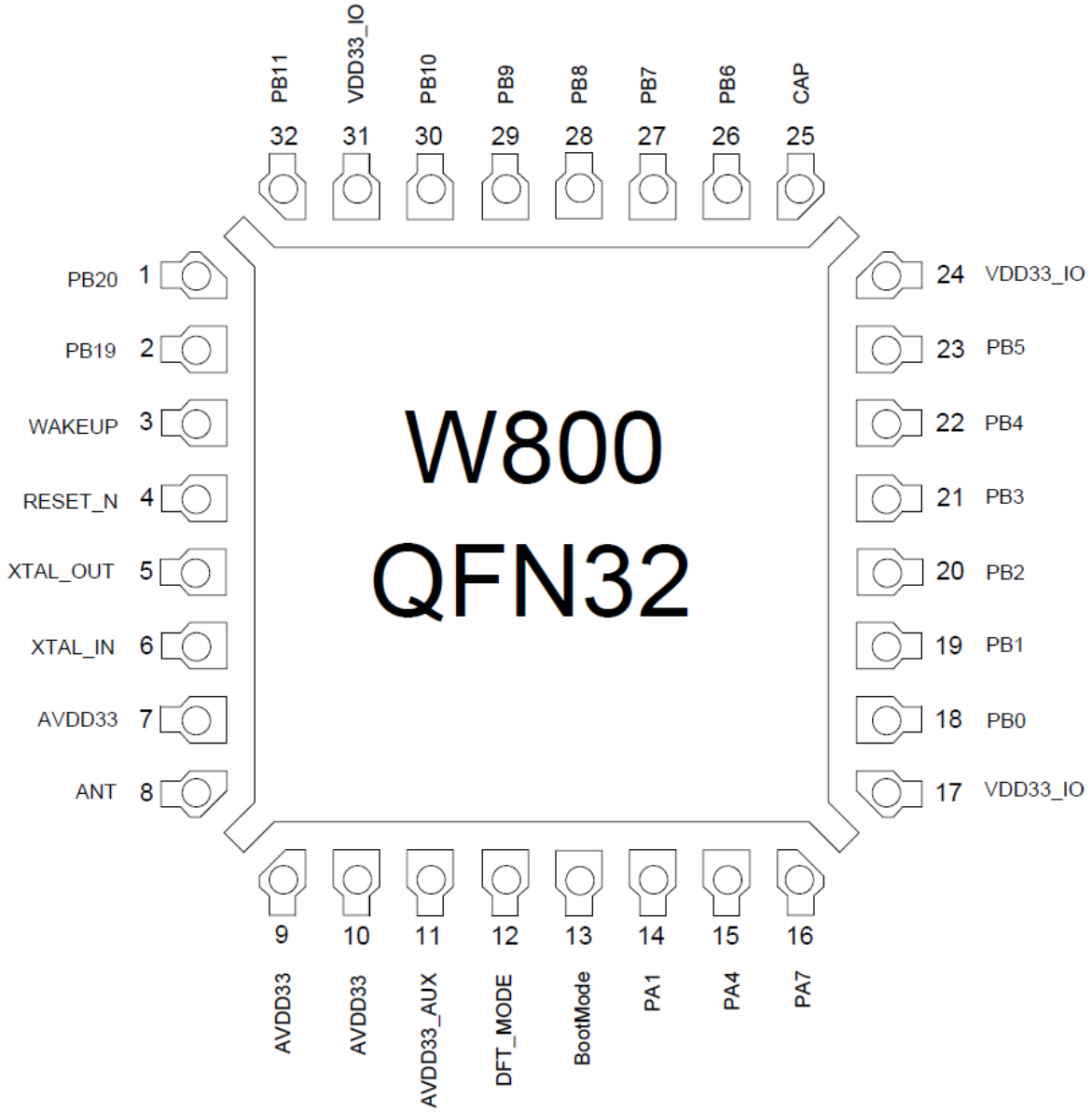

Figure6-1 W800 Pin Diagram (QFN32)

Table6-1 Pin Description (QFN32)

No.	Name	Type	Function Afer Reset	Multi-function	Max Frequency	Power of pull high/low	Driving Power
1	PB_20	I/O	UART_RX	UART0_RX/PWM1/UART1_CTS/I²C_SCL	10MHz	UP/DOWN	12mA
2	PB_19	I/O	UART_TX	UART0_TX/PWM0/UART1_RTS/I²C_SDA	10MHz	UP/DOWN	12mA
3	WAKEUP	I	WAKEUP			DOWN	

4	RESET	I	RESET			UP	
5	XTAL_OUT	O	Output external crystal oscillator				
6	XTAL_IN	I	Input external crystal oscillator				
7	AVDD33	P	Power supply, 3.3V				
8	ANT	I/O	RF antenna				
9	AVDD33	P	Power supply, 3.3V				
10	AVDD33	P	Power supply, 3.3V				
11	AVDD33_AUX	P	Power supply, 3.3V				
12	TEST	I	Test pin				
13	BOOTMODE	I/O	BOOTMODE	I²S_MCLK/LSPI_CS/PWM2/I²S_DO	20MHz	UP/DOWN	12mA
14	PA_1	I/O	JTAG_CK	JTAG_CK/I²C_SCL/PWM3/I²S_LRCK/ADC0	20MHz	UP/DOWN	12mA
15	PA_4	I/O	JTAG_SWO	JTAG_SWO/I²C_SDA/PWM4/I²S_BCK/ADC1	20MHz	UP/DOWN	12mA
16	PA_7	I/O	GPIO, input, high resistance	PWM4/LSPI_MOSI/I²S_MCK/I²S_DI /Touch0	20MHz	UP/DOWN	12mA
17	VDD33IO	P	IO power supply, 3.3V				
18	PB_0	I/O	GPIO, input, high resistance	PWM0/LSPI_MISO/UART3_TX/PSRAM_CK/Touch3	80MHz	UP/DOWN	12mA
19	PB_1	I/O	GPIO, input, high resistance	PWM1/LSPI_CK/UART3_RX/PSRAM_CS/Touch4	80MHz	UP/DOWN	12mA
20	PB_2	I/O	GPIO, input, high resistance	PWM2/LSPI_CK/UART2_TX/PSRAM_D0/Touch5	80MHz	UP/DOWN	12mA
21	PB_3	I/O	GPIO, input, high resistance	PWM3/LSPI_MISO/UART2_RX/PSRAM_D1/Touch6	80MHz	UP/DOWN	12mA
22	PB_4	I/O	GPIO, input, high resistance	LSPI_CS/UART2_RTS/UART4_TX/PSRAM_D2 /Touch7	80MHz	UP/DOWN	12mA
23	PB_5	I/O	GPIO, input, high resistance	LSPI_MOSI/UART2_CTS/UART4_RX/PSARM_D3/Touch8	80MHz	UP/DOWN	12mA
24	VDD33IO	P	IO power supply, 3.3V				
25	CAP	I	External capacitance, 4.7μF			-	
26	PB_6	I/O	GPIO, input, high resistance	UART1_TX/MMC_CLK/HSPI_CK/SDIO_CK/Touch9	50MHz	UP/DOWN	12mA
27	PB_7	I/O	GPIO, input, high resistance	UART1_RX/MMC_CMD/HSPI_INT/SDIO_CMD/ Touch10	50MHz	UP/DOWN	12mA
28	PB_8	I/O	GPIO, input, high resistance	I²S_BCK/MMC_DO/PWM_BREAK/SDIO_DO/ Touch11	50MHz	UP/DOWN	12mA

29	PB_9	I/O	GPIO, input, high resistance	I²S_LRCK/MMC_D1/HSPI_CS/SDIO_D1/ Touch12	50MHz	UP/DOWN	12mA
30	PB_10	I/O	GPIO, input, high resistance	I²S_DI/MMC_D2/HSPI_DI/SDIO_D2	50MHz	UP/DOWN	12mA
31	VDD33IO	P	IO power supply, 3.3V				
32	PB_11	I/O	GPIO, input, high resistance	I²S_DO/MMC_D3/HSPI_DO/SDIO_D3	50MHz	UP/DOWN	12mA
33	GND	P	Ground				

Note: 1. I = Input, O = Output, P = Power

7 Parameters

7.1 Ultimate Characteristics

Table7-1 ultimate characteristic

Parameter	Symbo	Min	Typ	Max	Unit
VDD supply voltage	VDD	3.0	3.3	3.6	V
Input low voltage	V_{IL}	-0.3		0.8	V
Input high voltage	V_{IH}	2.0		VDD+0.3	V
Input capacitance	C_{pad}			2	pF
Output low voltage	V_{OL}			0.4	V
Output high voltage	V_{OH}	2.4			V
Max output current	I_{MAX}			24	mA
Storage temperature	T_{STR}	-40℃		+125℃	℃
Operating temperature	T_{OPR}	-40℃		+85℃	℃

7.2 RF power parameters

Test conditions: 3.3V power supply, lauch test at 50% duty cycle.

表 7-2 射频功耗参数

Operation Mode	Typ	
TX IEEE802.11b 1Mbps POUT = +19.4dBm	240	mA
TX IEEE802.11b 11Mbps POUT = +19.3dBm	240	
TX IEEE802.11g 54Mbps POUT = +14.7 dBm	190	mA
TX IEEE802.11n MCS7 POUT = +12dBm	180	mA
RX IEEE802.11b/g/n	95	mA

7.3 Wi-Fi RF

Table7-3 Wi-Fi RF Parameters

Parameter	Typ	Unit
Input frequency	2.4~2.4835	GHz
TX Power		
IEEE802.11b 11Mbps	19±2	dBm
IEEE802.11g 54Mbps	16±2	dBm

IEEE802.11n MCS7 HT20	13±2	dBm
Sensitivity		
IEEE802.11b 1Mbps	-93	dBm
IEEE802.11b 11Mbps	-87	dBm
IEEE802.11g 54Mbps	-73	dBm
IEEE802.11g MCS7 HT20	-71	dBm
Adjacent Channel Restrain		
IEEE802.11b 6Mbps	32	dB
IEEE802.11g 54Mbps	16	dB
IEEE802.11n HT20, MCS0	31	dB
IEEE802.11n HT20, MCS7	12	dB

7.4 Bluetooth RF

7.4.1 Standard BT RF

Receiver-(Basic Rate)

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity @0.1% BER			-91		dBm
Max Received Signal @0.1% BER			0		dBm
Adjacent channel selectivity C/I			9		dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz		-10		dBm
	2000 MHz ~ 2400 MHz		-27		dBm
	2500 MHz ~ 3000 MHz		-27		dBm
	3000 MHz ~ 12.5 GHz		-10		dBm
Intermodulation			-39		dB

Transmitter (Basic Rate)

Parameter	Condition	Min	Typ	Max	Unit
RF transmit power			6		dBm
Gain control step			3		db
RF power control range		-10		12	dBm
20 dB Bandwidth		0.918	0.923		

Δ f1avg			159.8		
Δ f2max			142.8		
Δ f2avg/Δ f1avg			0.89		
ICFT			0		
Drift rate		-2.25	-2.08	2.23	kHz
Drift (DH1)		-4		-1	kHz
Drift (DH5)			0	21	kHz

Receiver (Enhanced Data Rate)

Parameter	Condition	Min	Typ	Max	Unit
π/4 DQPSK					
Sensitivity @0.01% BER			-88		dBm
Max Received Signal @0.01% BER			0		dBm
8DPSK					
Sensitivity @0.01% BER			-81		dBm
Max Received Signal @0.01% BER			0		dBm

Transmitter (Enhanced Data Rate)

Parameter	Condition	Min	Typ	Max	Unit
RF transmit power			0		dBm
Gain control step			3		db
RF power control range		-10		8	dBm
π/4 DQPSK max w0		-3.2		2.6	KHz
π/4 DQPSK max wi		-5.3		-2.4	KHz
π/4 DQPSK max |wi + w0|		-4.8		-3.9	KHz
8DPSK max w0		-1.4		1.5	KHz
8DPSK max wi		-4.1		-2.9	KHz
8DPSK max |wi + w0|		-4.8		-4.1	KHz
π/4 DQPSK	RMS DEVM		6.7		%
	99% DEVM		100		%
	Peak DEVM		14.1		%
8 DPSK	RMS DEVM		6.8		%
	99% DEVM		99.99		%
	Peak DEVM		15.3		%
EDR differential phase coding			100		%

7.4.2 BLE RF

Receiver

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity @30.8% PER			-94		dBm
Maximum reveived signal @30.8% PER				0	dBm
Out-of-band blocking performance	30MHz~2000MHz		-30		dBm
	2003MHz~2399MHz		-35		dBm
	2484MHz~3000MHz		-35		dBm
	3000MHz~12.5GHz		-30		dBm
Intermodulation			-47		dBm

Transimitter

Parameter	Condition	Min	Typ	Max	Unit
RF transmit power			6		dBm
Gain control range			2		db
Adjacent channel transmit power		-10		12	dBm
Δ f1avg		240.8	241.2	242	kHz
Δ f2max		175.7	182.7	183.9	kHz
Drift rate			1.5		kHz
Drift			-4.3		kHz

8 Package Mechanical

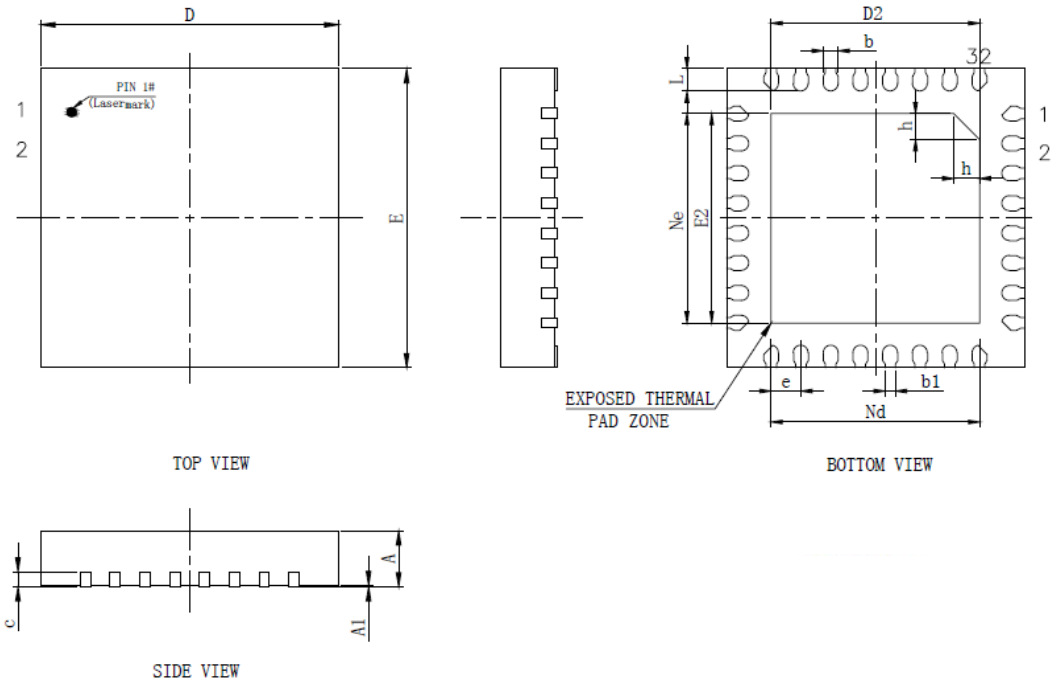

Figure8-1 W800 package outline

Table8-1 W800 package mechanical data

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.40BSC		
Ne	2.80BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40
L/F carrier size	122x122		